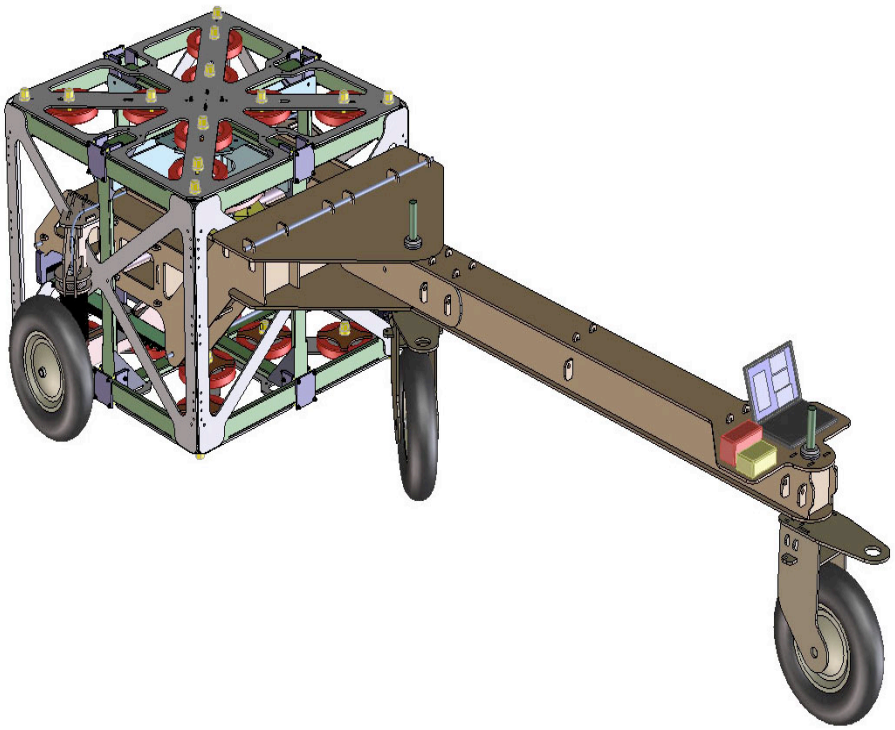
UXO Engineering Design

Technical Specification

and

Conceptual Design



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1. Introduction

The design and fabrication of the UXO detector has numerous challenges and is an important component to the success of this study. This section describes the overall engineering approach, as well as some of the technical details that brought us to the present design.

In general, an array of sensor coils is measuring the signal generated by the UXO object in response to a stimulation provided by the driver coil. The information related to the location, shape and properties of the object is derived from the analysis of the measured data. Each sensor coil is instrumented with a waveform digitizer operating at a nominal digitization rate of 100 kSamples per second. The sensor coils record both the large transient pulse of the driver coil and the UXO object response pulse. The latter is smaller in amplitude and must be extracted from the large transient signal. The resolution required is 16 bits over a dynamic range of at least 140 dB. The useful signal bandwidth of the application extends from DC to 40 kHz. The low distortion of each component is crucial in order to maintain an excellent linearity over the full dynamic range and to minimize the calibration procedure.

The electronics must be made as compact as possible so that the response of its metallic parts has a minimum signature response. Also because of a field system portability requirement, the power consumption of the instrument must be kept as low as possible.

2. Summary of specifications, requirements and goals

The following summarizes the most relevant requirements for the design and fabrication of each element of the system.

Cart:

- Non-magnetic, non-metallic
- Smooth ride
- Damping is good, more is better.
- One-man operation, push or pull.
- Fits through the laboratory door.
- Must have adjustability to accommodate real masses and observed sensitivity to disturbances.

Electronics:

- Sampling rate: >100 kS/s
- Dynamic range: >160 dB
- Battery operation - > 2hrs125
- Capability of vibration measurements
- Capability of GPS positioning of the system

Signal processing:

- Data processing to detect a device in the required processing time
- Easy to use interface
- Data processing capabilities both on-board and on the local computer

General requirements:

- Easy to maintain and transport
- Easy to install
- Portable

3. System requirements and description

The main system requirements to guide the engineering approach to the design and fabrication of the device are summarized in the next section. .

Due to the nature of the device, it is important to minimize the metallic content of the structure: all elements are made out of a combination of wood, plastics and fiberglass. The only areas with conductors, besides the driving and sensing coils, are going to be the associated with the data acquisition system, which will be positioned at such distance from the driver/receiver cube that will have no effect on the data acquisition.

In addition, the system will be equipped with and powered by a battery capable of running the whole system from pulsing to recording data for a minimum of two hours. Appendix 1 provides the basic calculations for the battery lifetime.

A critical design decision is that to wire the sensors directly into the data acquisition system as opposed to processing the signals at the sensors and transmitting the resulting data via air or fiber optic. The choice of wiring the sensors allows a simplified installation and electronics configuration, and requires that the pre-amplifiers first seen by the sensor coils present a high impedance to prevent current flows that could be induced by the excitation field and result in measurement errors.

One of the main challenges to the data acquisition system is the very large dynamic range. This is driven by the specifications described earlier. Using $2nV/\sqrt{Hz}$ as the nominal performance of low noise amplifiers, one can calculate the noise floor of a good front-end amplifier to be at least 1 μV = $2\text{nV} \times \sqrt{200\ \text{kHz}}$, assuming a 200 kHz noise band. The resulting amplitude of the excitation pulses corresponds to peak-to-peak voltages in excess of 100 V. The resulting dynamic range, in excess of 160 dB is achieved by a combination of active switching and sensor configuration. Part of this dynamic range is provided by the configuration of the sensors and their location, where symmetry through the center of the system allows for cancellation of the primary fields and ambient noise while the secondary fields from the target are easily measured in the differenced output. We have measured a drive signal cancellation of about 50:1.

The choice of noise floor was carefully made to consider all sources. In particular, we selected low noise pre-amplifiers and established their expected noise floor. We then designed sensing coils to have an intrinsic noise below that of the amplifiers, so that the sensors would not be the limiting factors. A full characterization of the system noise was made in several configurations, from a single sensor, to the full 8 sensor pairs.

Particular attention is also required to ensure the portability of the system, not only does it need to move and scan across fields, but it needs to be easily transported, assembled and maintained. The reactive parts of the coil (L and C) are to first order noiseless. The only noise source associated with the coil is its damping resistor. However the reactive parts are contributing indirectly because of the resonance that they produce.

4. System description

The system block diagram is shown in Figure 1. A logic board controls the drivers for the three coils that excite each of the three planes. The same board also triggers the data acquisition system, selects and pre-processes the data and interfaces with the main local computer system.

Particular care is given to the grounding of the system and its relation with drivers and sensors, to minimize undesired noise.

A local computer is connected via the USB port to the logic board. Such computer is going to initially perform all data processing, including the visualization of the results. The USB link has been successfully tested to transfer data at a speed of 33 MB/s, thus allowing for the direct transfer of data taken by all channels at 16-bit resolution when digitizing at the full 500 kS/s. The current system limitation is the ability of the local computer to receive and process this data in real time.

We are therefore planning to have two modes of acquisition, one at standard resolution, and one at high resolution. In standard mode, stacking of multiple shots will be performed on board, and then passing on the processed data to the local computer. When the data processing on the computer requires the complete dataset, the duty factor of the drivers will be reduced, thus limiting the in-flow of data while maintaining the data transfer rate to the local computer through the USB interface. This will allow more time for the local computer to process the data and display information in real time.

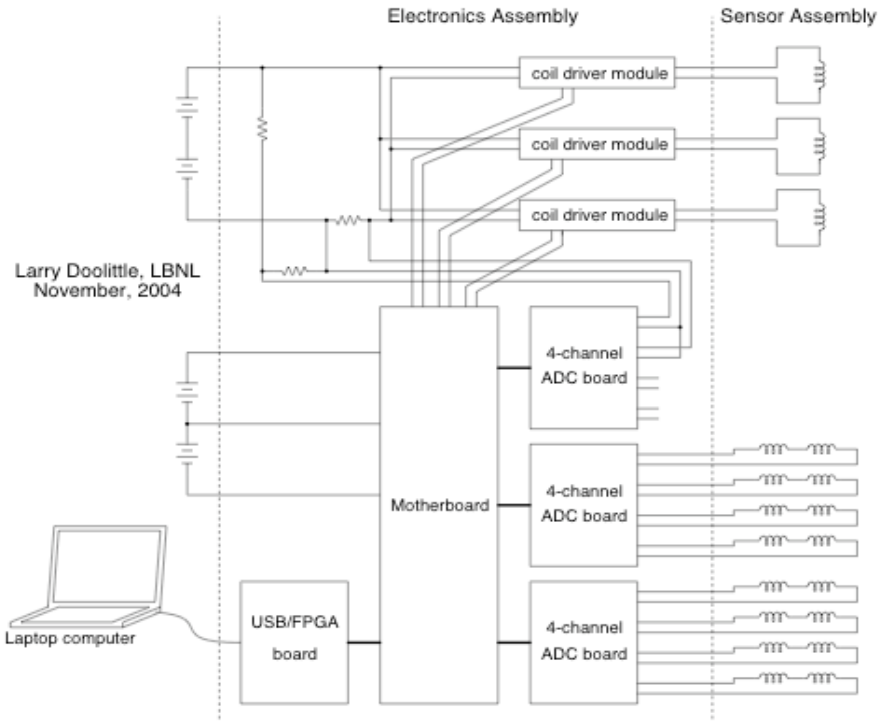


Fig. 1 – Overview of the system architecture

5. Data Acquisition and Processing System

The heart of the system is an FPGA-driven embedded processor. This programmable smart chip will drive all timing and system synchronization, interface with the data acquisition boards and after receiving the digital data, it will process and store in on-board DDRAM. This FPGA will manage the data transfer to the main computer where the data will be stored in large sizes and displayed. Among the timing information generated, the processor will provide triggers for the pulsers, as well as gain switching information to the data acquisition system.

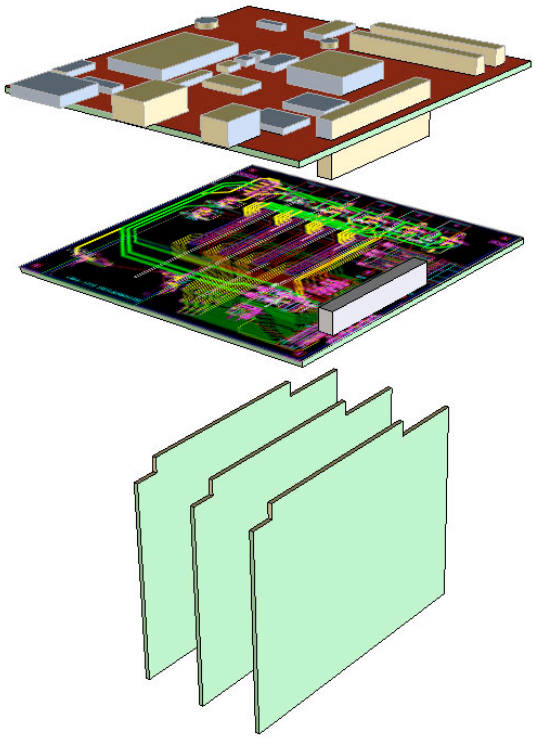


Fig. 2 – Exploded view of the data acquisition system prototype

In order to minimize expenses and expedite system development, we adopted a standard development board based upon the Xilinx Virtex IV FPGA. This board (shown in red in Fig. 2) provides readily available network and USB connections, and allows for easy and simple loading of FPGA firmware on board. It also contains a boot memory chip to load firmware on power-up. The logic board interfaces with a

custom developed motherboard that carries all the power supply regulation and receives up to 4 four-channel data acquisition cards. Only three are shown in Fig. 2, since we are currently planning to instrument only 12 channels and leave the extra capacity available for future expansion. The data acquisition chain is based on 16-bit digitizers capable of sampling up to 500 kS/s and described in detail in Chapter 14, together with the design of the low-noise analog front end signal processing.

6. Engineering approach

We have taken a step-wise approach to the engineering of the device. On one side, we want to arrive to experimental results as early as possible, on the other we do not want to compromise the chance of making an easy transition to a final design that can be transferred to industry for production and distribution. As a result, we have been using two 4-channel oscilloscopes to acquire data from the 8 sensor pairs, and the memory built in the scopes for stacking and averaging up to 100 acquisition events. This data is taken at 8 bits in the identical setup, which was used to collect the experimental data with the previous, proof-of-principle system. The proof-of-principle system was much simpler and based upon smaller sensors that were not paired up to leverage the cancellation of the drive pulse. In the meantime we are developing the 16-bit custom electronics with gain switching which will provide much better resolution and dynamic range.

At present we have completed the data acquisition at 8 bits and have started the bench tests of the 16-bit system with gain switching. The comparison with previous data indicated an improvement of approximately one order of magnitude in device resolution.

A similar approach is planned for the firmware implementation, where we intend to add features and functionality incrementally, and slowly move on chip many of the functions and operations that we will be performing at first on the local computer.

7. System Modeling

In order to develop a good understanding of the system and a useful analytical tool, we modeled the system both with a mathematical model and with an equivalent circuit. Both models reflect the mutual coupling between drivers and objects, and include the first stage of analog processing. In the equivalent circuit we could also study noise behavior. A simplified circuit of a whole system (transmitter, receiver, and target) is shown in Fig. 3.

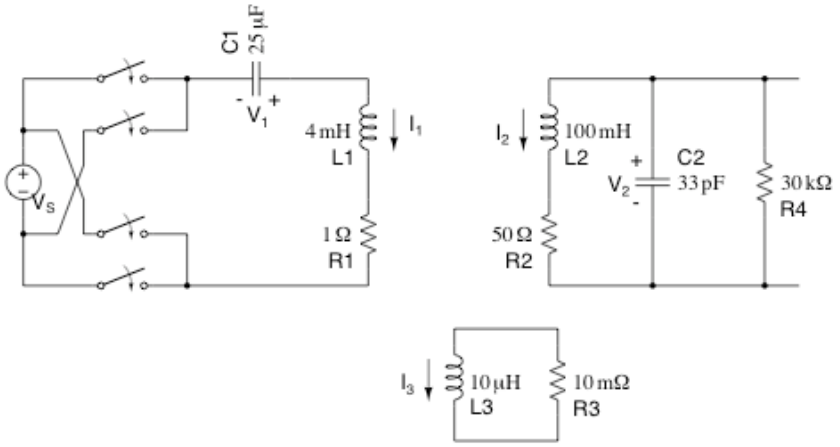


Fig. 3 – Simplified circuit diagram

The relationship between circuit components is governed by following equations:

$$L_1 \frac{dI_1}{dt} + M_{12} \frac{dI_2}{dt} + M_{13} \frac{dI_3}{dt} = V_1 - I_1 R_2 \tag{1}$$

$$C_1 \frac{dV_1}{dt} = -I_1 \tag{2}$$

$$M_{12} \frac{dI_2}{dt} + L_2 \frac{dI_2}{dt} + M_{23} \frac{dI_3}{dt} = V_2 - I_2 R_2 \tag{3}$$

$$C_2 \frac{dV_2}{dt} = -I_2 - \frac{V_2}{R_4} \tag{4}$$

$$M_{13} \frac{dI_3}{dt} + M_{23} \frac{dI_2}{dt} + L_3 \frac{dI_3}{dt} = -I_3 R_3 \tag{5}$$

Which fits the formalism

$$A \frac{d\vec{Y}}{dt} = B\vec{Y} \tag{6}$$

Defining $C = A^{-1} B$, we get the simpler form:

$$\frac{d\vec{Y}}{dt} = C\vec{Y} \tag{7}$$

It is then easy to write the solution to this equation in terms of eigenvalues and eigenvectors of C.

An example of the result of a simulation from this model is shown in Fig. 4.

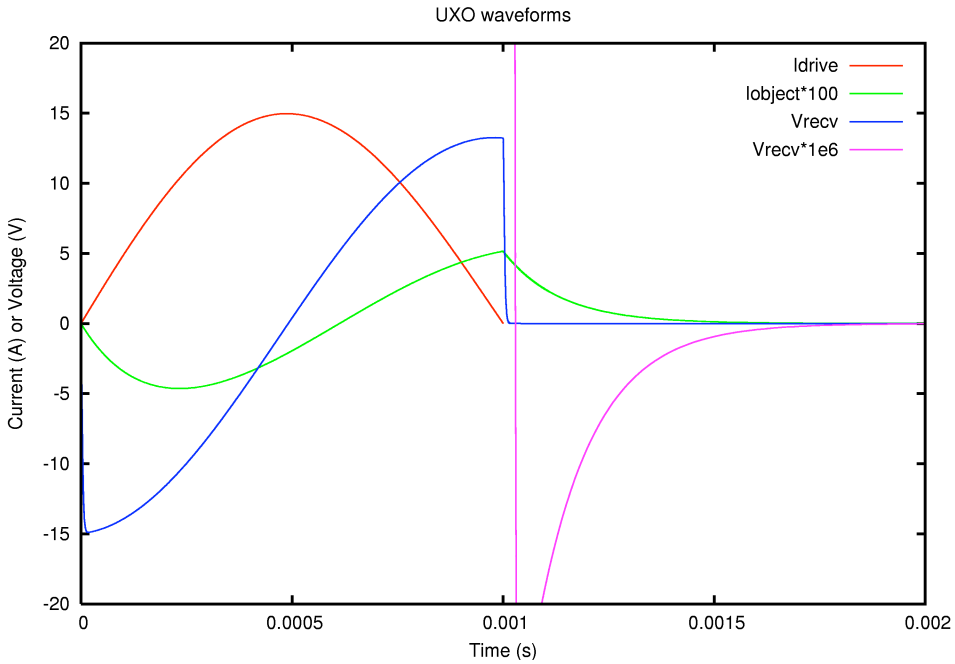


Fig. 4 – Model output for given parameter set

which was calculated by using the following parameters:

$L_1 = 4$ mH,

$L_2 = 10$ mH,

$L_3 = 10$ μH,

$C_1 = 25.3$ μF,

$C_2 = 33$ pF,

$R_1 = 1$~Ω,

$R_2 = 50$ Ω,

$R_3 = 0.075$ Ω,

$R_4 = 27.4$ kΩ,

$M_{12} = 3 \times 10^{-4}$,

$M_{13} = 10^{-7}$,

$M_{23} = 10^{-7}$.

8. Transmitter (Driver) Design

The driver is made of separate coils that transmit a magnetic pulse in each of the three planes. The horizontal driver is split in two coils to ensure symmetry around the sensor. Much like the sensing coils, the design of the transmitters is a compromise between size, number of turns, induced voltage and exciting field. In this case total weight and current capacity are also important considerations. The following represents the measurement result of the existing driver coils as built. With the present 24V battery setup, this transmitter is capable of 60 A pk-pk, which would induce a transient voltage of up to 1500 V pk-pk.

X plane:

L_X = 2.86 mH. 36 turns of # 12 AWG wire,

The coil is 6.5 lbs. and 37 3/4" x 28”, and is mounted on the outside in a vertical position.

Y plane:

L_Y = coil 3.1 mH, 36 turns of #13 AWG wire;

The coil is 6.4 lbs. and 37 3/4" x 26 3/4” and is mounted on the inside in a vertical position.

Z plane:

Upper L_HU = 1.4 mH, 22 turns of #12 AWG wire:

Lower L_HL = 1.4 mH, 22 turns of #12 AWG wire

L_HT = 3.0 mH - when added in series for a total of 44 turns of #12 AWG wire

The weight of the horizontal coils combined is 16 lbs; each coil and frame is 39 1/8" square.

The pulser electronics is based on a half-sine generated by resonating a capacitor with the inductance of the drive loops. SCR rectifier switches, triggered by the logic board, control the waveform and are optimized to prevent bouncing of undesired effects from the turn-on or turn-off transients that could interfere with the detection of UXOs.

Fig 5 below shows the electronics used to drive each channel. The triggering and timing distribution system is provided by the FPGA, while each pulse is being monitored and recorded by the data acquisition system, to allow for comparison, calibration and improved data analysis.

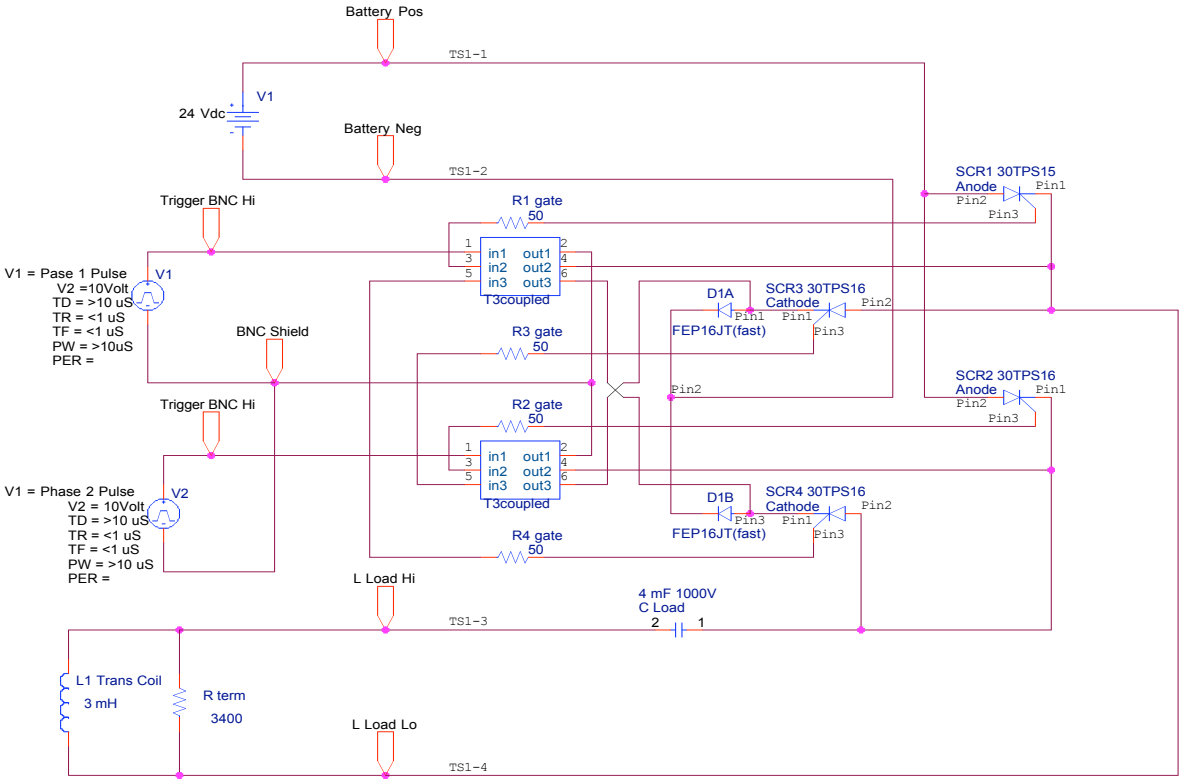


Fig. 5 – Electronic transmitter circuit diagram

9. Conceptual design of the sensors

The sensors are critically damped loops, resonant at 20 kHz by the addition of an adjustable external capacitance. The final choice of diameter, wire size, and number of turns was a compromise between sensitivity, self-resonance, internal resistance, and resolution. In the end, we settled for 6" ID, 500 turn sensors. While a larger diameter results in a higher sensitivity, it also reduces resolution as the signals are more distributed. Likewise, more turns offer a stronger signal, but lower the coil's self resonance which needs to remain above the desired operating band.

Particular care is needed when tuning sensors, both individually and as a sensor pair. We built a board containing all passive networks used for tuning and critically damping. Each sensor is first tuned and individually damped. Then the sensors are paired, and their shields connected together to ground, while a balancing capacitor is added. All adjustments are done at board level. All sensor pairs measured very close to each other. The schematic of the tuning of a single coil pair is shown in Fig. 6.

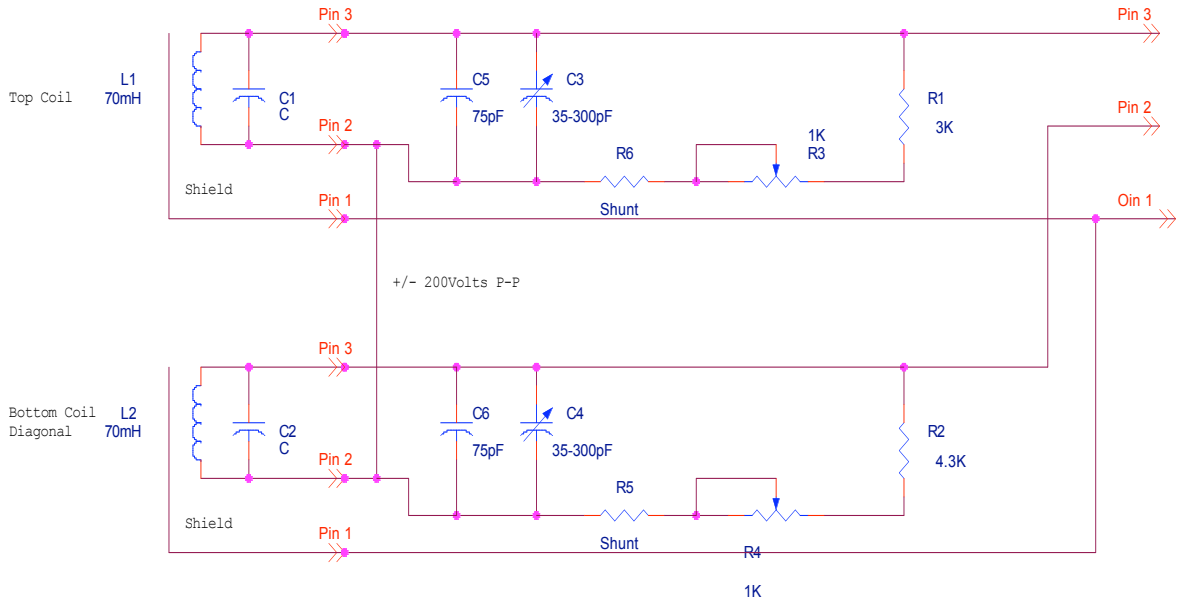


Fig. 6 – Sensor pair tuning and matching network

10. Sensor fabrication

The sensors are fabricated using a Delrin spool and winding formvar wire into the spool (Fig. 7). After winding, an aluminum foil/ fiberglass tape is insulated/layered and provides a non-shorting shield. An additional tape layer is the final covering. The coil ties to a 3 pin plug:1-shield, 2-coil inner lead, 3-outer coil lead. The RLC network is tuned to resonate at 20 kHz and then critically damped.

Reference parameters from actual sensor measurements are as follows:

- 6" inner radius, 3/4" wide, 500 turns #26 formvar wire, wound on a Delrin spool.
- R ~ 35 Ω, L ~70 mH,
- instrinsic resonance frequency ~65 kHz (with 10 foot shielded twisted pair).

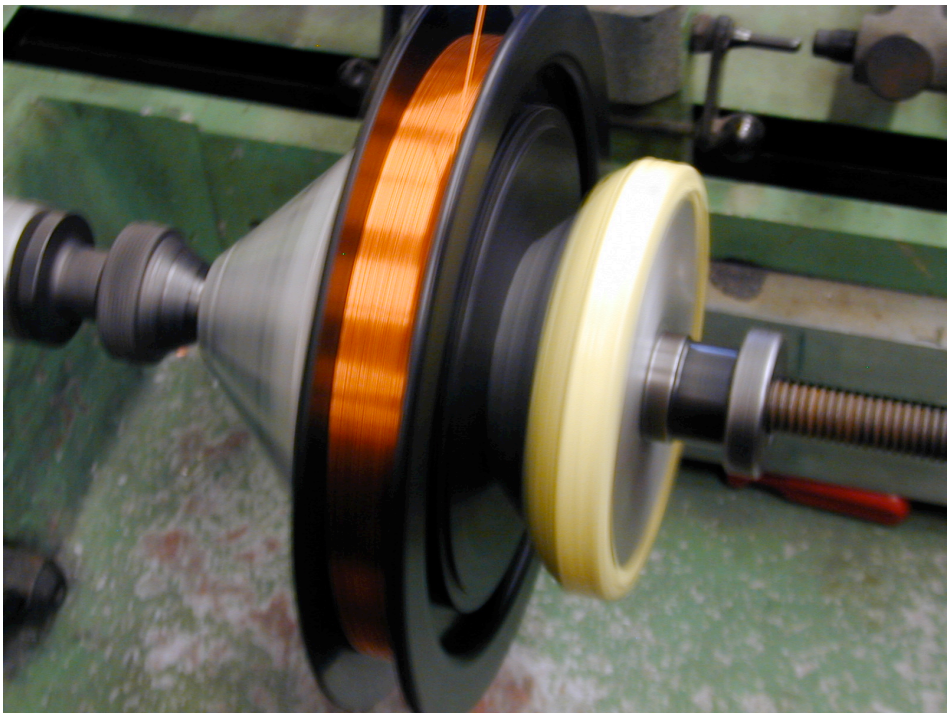


Fig. 7 – Sensor winding setup

11. Electronics design

The following sections describe in detail the design and development of the electronics processing system that is necessary to achieve the specified dynamic range and necessary to support the resolution required in the detection of the UXO targeted in this project.

We approached the problem in phases, starting from the analysis and selection of the low noise amplifiers for the front end, to the modification of an existing digital to analog converter board for data acquisition, to the implementation of an FPGA-based evaluation board to ensure data capture and interface with an external computer.

Testing each step separately, we were able to evaluate each component of the signal processing chain and make the necessary adjustments, without the need to have a complete, functional system. This approach led to the existing design which will allow us to test the data with the required dynamic range, and be the base for the final system design.

The following sections will describe each step of the chain in detail, starting from the design of a single channel front end.

12. Simplified Channel Architecture

The simplified channel architecture is depicted in Fig. 8.

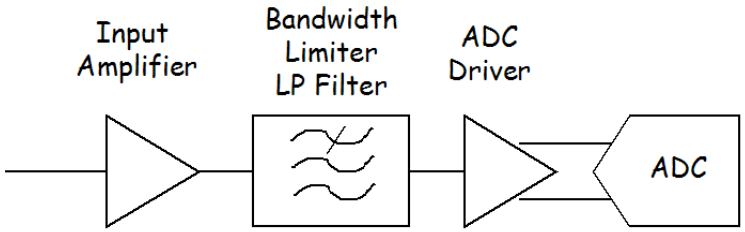


Fig. 8 : Simplified Channel Architecture.

The input amplifier choice is crucial for the overall noise performance of the system. The low-pass filter acts both as a noise bandwidth limiter and as an anti-aliasing filter. The Analog to Digital Converter (ADC) driver conditions the signal to match the input range of the ADC.

The critical parts of the above architecture are the input amplifier and ADC. Their selection is dictated by the noise and transient characteristics of the parts themselves in relation to the needs of the application.

13. Input stage amplifier

13.1. Noise Analysis

The input amplifier is a non-inverting amplifier. The sensor coil's signal is presented to the high-impedance input of the amplifier. As previously mentioned, the noise performance of the first stage is crucial for the performance of the entire system. The noise analysis is conducted according to the model depicted in Fig. 9.

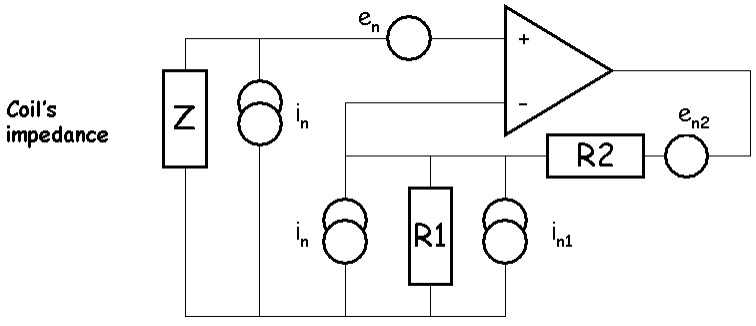


Fig. 9: Input Stage Model for noise analysis.

Introducing the following parameters:

- Z: Coil impedance (varies as function of frequency)
- e_n: input voltage noise density of the amplifier
- i_n: input current noise density of the amplifier
- i_{n1}: current noise density of the R_1 resistor
- e_{n2}: voltage noise density of the R_2 resistor
- $e_{0,out}$: output noise voltage density
- $e_{0,in}$: input referred noise voltage density

The calculation yields,

$$e_{o,out}^2 = \left(1+\frac{R_2}{R_1}\right)^2 \times e_n^2 + Z^2 \times \left(1+\frac{R_2}{R_1}\right)^2 \times i_n^2 + R_2^2 \times i_n^2 + 4kTR_2 + \frac{4kT}{R_1}R_2^2$$

$$e_{o,in}^2 = e_n^2 + Z^2 \times i_n^2 + \left(\frac{R_1 \times R_2}{R_1+R_2}\right)^2 \times i_n^2 + 4kT \times R_2 \times \left(\frac{R_1}{R_1+R_2}\right)^2 + 4kT \times R_1 \times \left(\frac{R_2}{R_1+R_2}\right)^2 \quad (8)$$

The input referred noise density has four components:

- The first one is the input voltage noise density of the amplifier.
- The second one shows that the input current noise density is multiplied by the coil's impedance, which presents a resonance at 20 kHz by design. This result yields to the selection of the input stage amplifier.
- The last two terms are related to the choice of gain-setting resistors.

13.2. Selection criteria for the input amplifier

Though the voltage input noise densities of bipolar-transistor-input operational amplifiers are comparable to those of Field Effect Transistor (FET) ones, the current input noise density characteristics of the latter are far lower by several order of magnitudes. As shown in the noise calculation (Eq. 8), the coil's impedance multiplies the input current noise density and that choice dictated the choice of the amplifier type. Other important characteristics taken into consideration were the power supply range and the output dynamic range, allowing for a large first stage gain, making the noise contributions of the subsequent stages negligible. Slew-rate, overdrive recovery and distortion were also considered.

We selected two FET-input amplifiers (OPA655 and OPA637 from the Texas Instruments/Burr Brown Corporation) and evaluated them on prototype boards.

13.3. Amplifier Selection

The tests that were performed confirmed that both amplifiers would meet the requirements for the application. We selected the OPA637 because its power supply range and its output dynamic range is wider. The following table summarizes the main characteristics of those amplifiers.

Parameter	**OPA655**	**OPA637**
Input Voltage Noise	20nV/√Hz @ 100Hz 8nV/√Hz @ 1kHz 6nV/√Hz @ >10kHz	15nV/√Hz @ 10Hz 8nV/√Hz @ 100Hz 5.2nV/√Hz @ 1kHz 4.5nV/√Hz @ 10kHz
Input Current Noise	1.3fA/√Hz @10Hz-10kHz	1.6fA @ 100Hz
Power Supplies Range	± 5V	± 15V
Output Dynamic Range	± 3.4V	± 12.5V
Gain Bandwidth Product	240MHz	80MHz
Slew Rate	> 200V/μs	> 120V/μs
Overdrive Recovery	< 10ns	< 500ns

Table 1: OPA655 and OPA637 Selected Characteristics.

13.4. Noise simulations

A SPICE model of the input circuit has been developed to complete the noise analysis with simulations. The model of the OPA637 contains all the necessary parameters to conduct the noise simulation.

A model of a 3-inch coil with a resonance frequency of 20 kHz has been included into the model and noise simulations have been conducted.

The input referred voltage noise density is shown in Fig. 10.

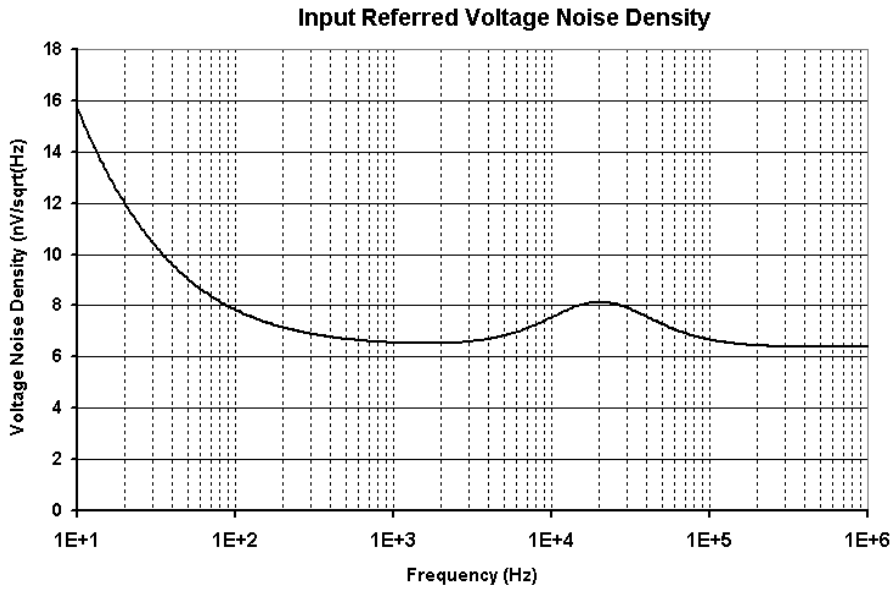


Fig. 10: Input Referred Voltage noise density (SPICE Simulation Result)

The influence of the coil's impedance mentioned in Chaper 13.1 is verified by those simulation results: the voltage noise density exhibits a peak at the resonance frequency of the coil.

13.5. Noise Measurements with a 3" coil

Noise measurements have been conducted with the prototype circuit and the 3-inch coil. Fig. 11 shows calculated and measured output voltage noise, and Fig. 12 shows the output voltage noise density.

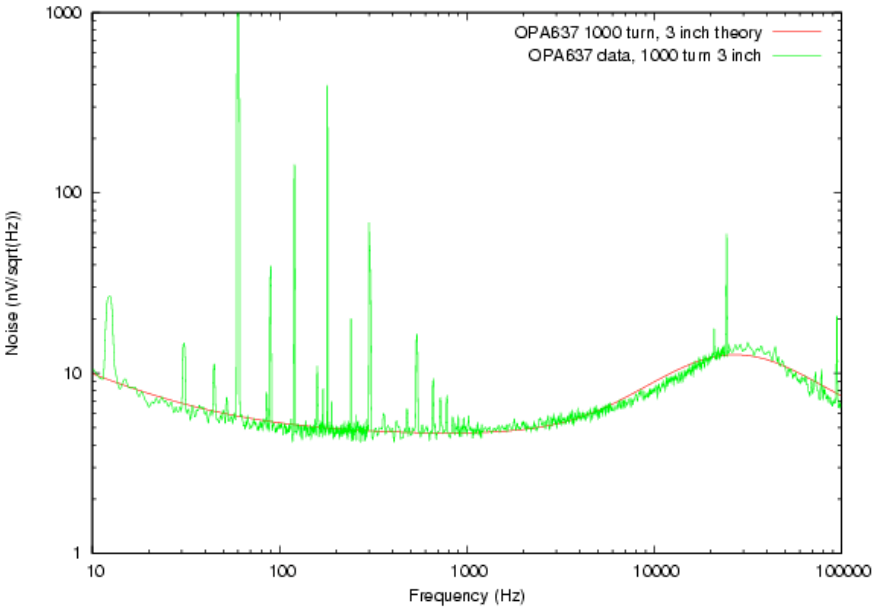


Fig. 11: Calculated and measured output voltage noise.

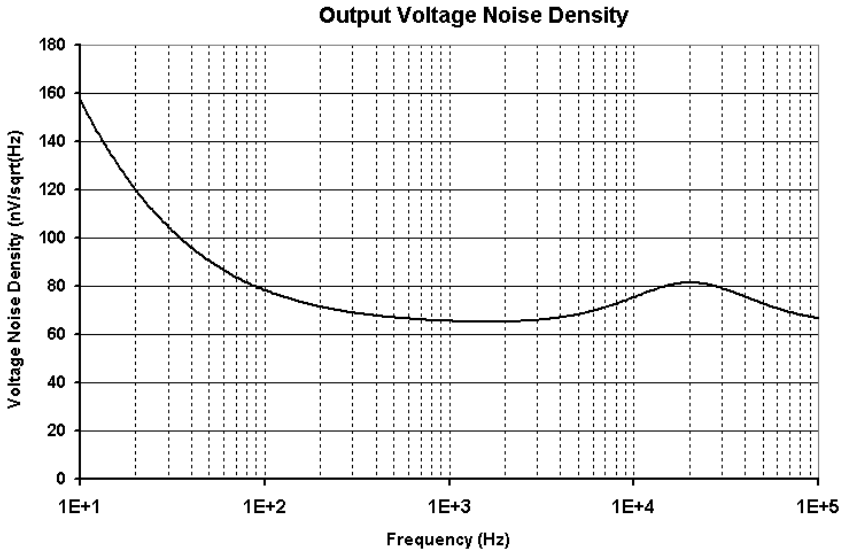


Fig. 12: Output Voltage noise density (SPICE Simulation Result)

14. Selection of the Analog to Digital Converter (ADC)

The resolution requirement of the application is 16-bit. Based on knowledge and experience from another similar design, the selected ADC is the Analog Devices AD7676 that has a resolution of 16-bits and a selectable sampling rate up to 500 kSamples/s. The functionality and the performance of the AD7676 were verified by using specifically developed prototype boards (Fig. 13).

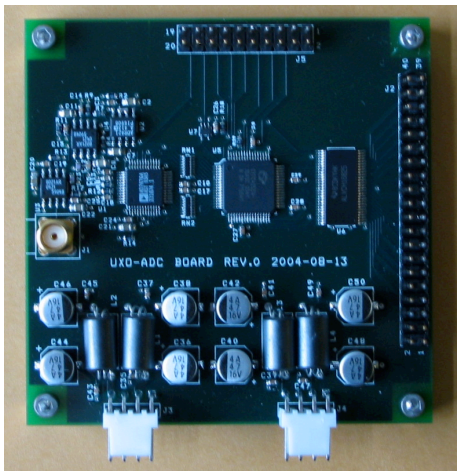


Fig. 13: AD7676 Prototype Board – Parallel Mode

The data acquisition and data transfer were performed through a specially developed micro-controller and USB interface board (Fig. 14).

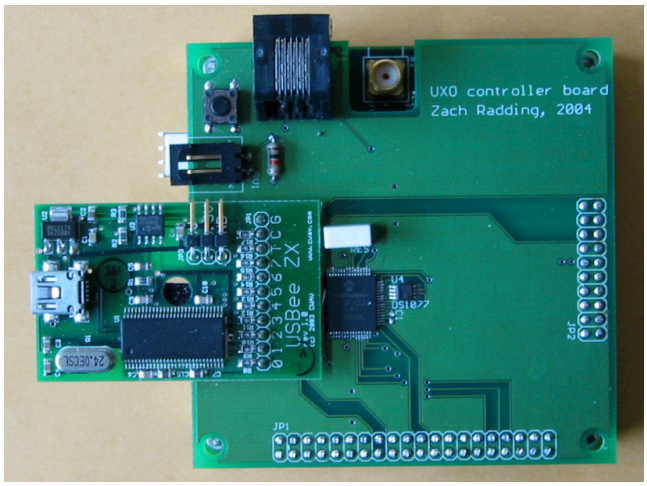


Fig. 14: AD7676 Data Acquisition and Transfer Prototype Board.

All the tests were conclusive and validated the choice of the AD7676.

15. Four-Channel Analog Signal Processing Board – UXO4CH

After selecting and verifying the functionality of the critical parts, those were included in the design of the four-channel prototype board. The modularity of the system was chosen to be four to optimize the numbers of channels versus the number of boards. The following sections of this paragraph detail the different part of the processing channel. The block diagram of the UXO4CH board is shown in Fig. 15.

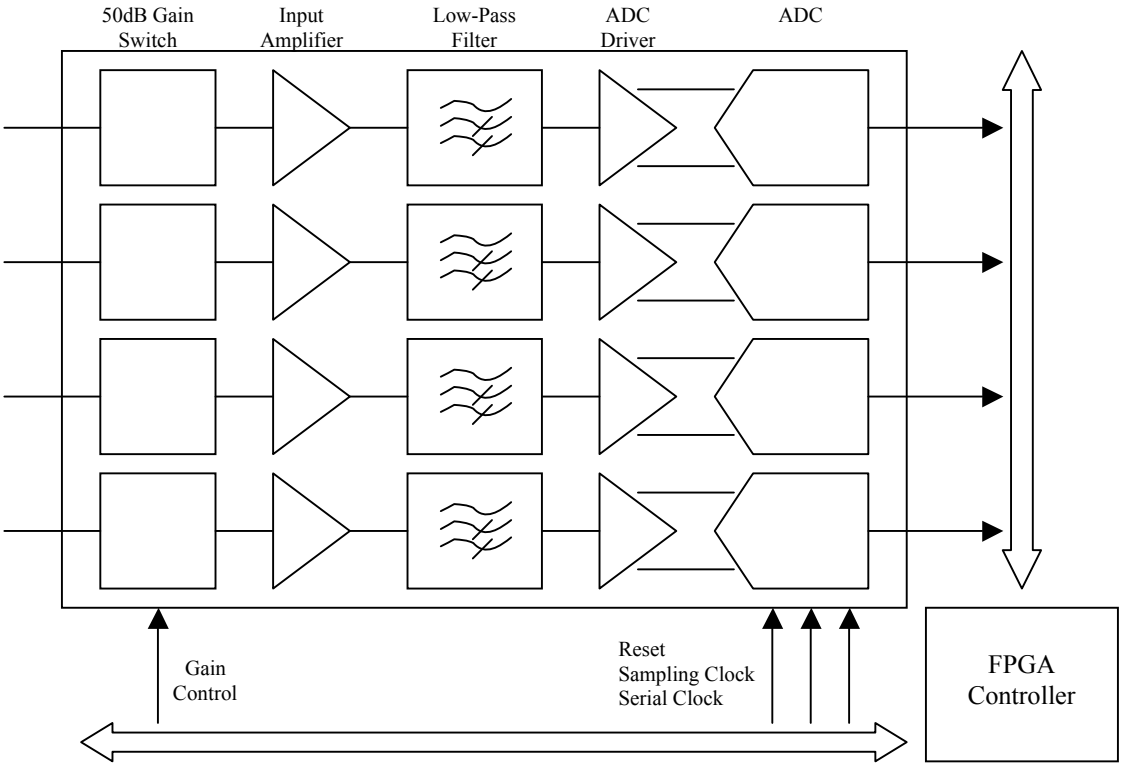


Fig. 15: UXO4CH Block Diagram

15.1. Input protection

Due to the potentially large transient signals that the sensor coils can record, the inputs of every channel have been protected by fast clamping diodes.

15.2. Dynamic Range and Gain Switch

In order to cover the large dynamic range required for the application, a gain switch circuit was included at the very input of the processing channel. The gain is selected through a control bit command issued by the FPGA board controller.

The nominal dynamic range of the ADC is 96 dB (16 bits). Through a 50 dB gain switch, the dynamic range of the instrument is extended to 146 dB. Fig. 16 shows the two gain ranges defined by the gain switch:

- The Low gain mode, for large transient signal from the driver coil
- The High Gain/High resolution mode for the UXO signals.

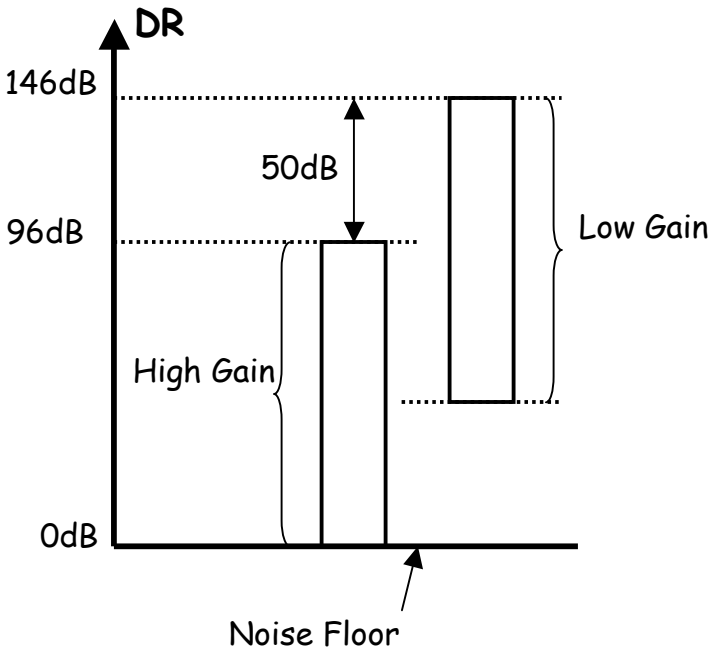


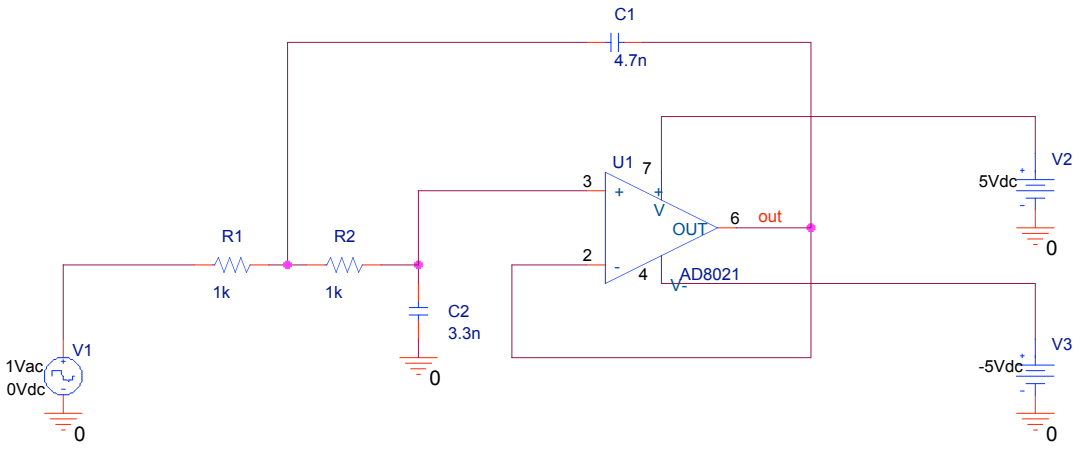
Fig. 16: Gain Switch and Dynamic Range

15.3. Input Amplifier

Most of the information related to this part of the circuit has been discussed in paragraph 4XXThe input amplifier is an operational amplifier in the non-inverting configuration. The amplifier is the OPA637 and the gain was set to +10. The power supplies are +/-12V.

15.4. 40 kHz Low Pass Filter

The importance of limiting the signal bandwidth is to obtain both a limitation of the noise bandwidth and an anti-aliasing function at the same time. A two-pole Bessel-type low-pass filter was selected since it provides the least amount of distortion. The two-pole structure was implemented using a Sallen-Key structure built around a low-noise and low-distortion amplifier. The schematic and Bode Gain plot are shown in Figs. 17 and 18.




```
C1 = 4700 pF
C2 = 3300 pF
R1 = R2 = 1000 Ohm
Q  = 0.597
f0 = 40.4 kHz
```

Fig. 17: Two-pole low-pass Bessel Filter – Sallen-Key Architecture

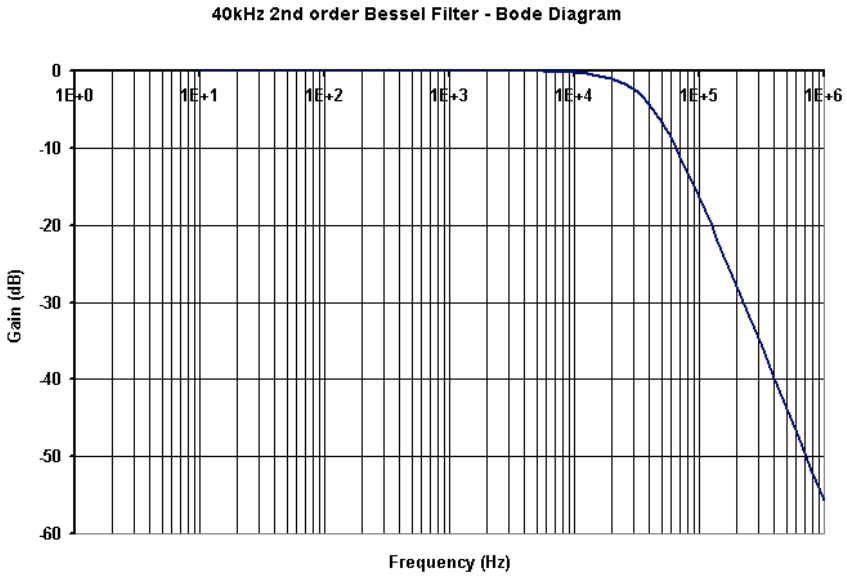


Fig. 18: Two-pole low-pass Bessel Filter – Bode Gain plot.

15.5. ADC Driver

The ADC driver is a single-ended-to-differential driver (Fig. 19) that also offsets the signal so that the ADC can record the bipolar signals provided by the sensor coils.

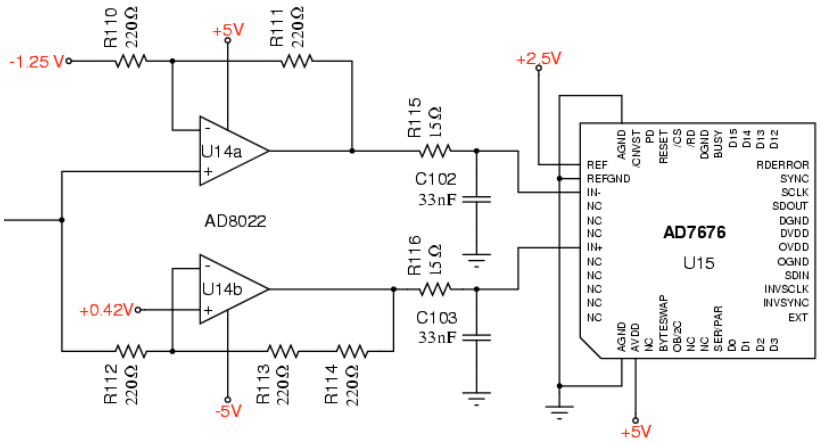


Fig. 19: Single-ended-to-differential Amplifier

The single-ended-to-differential amplifier is built around the AD8022 (dual version of the AD8021). This stage provides 6 dB of signal amplification. Additional filtering is provided in the signal path by two low-pass filters. The common-mode of the differential signal is set through the two reference voltages.

15.6. Voltage Reference

A single low-noise low-drift voltage reference was selected to provide the reference levels to the ADC and to the single-ended-to-differential driver. Appropriate buffering and filtering was provided to ensure the proper distribution and decoupling of the reference voltage. The single-ended-to-differential levels are generated at the channel level.

15.7. Analog to Digital Converter

All four ADCs are simultaneously operating. The conversion cycle and the data transfer is fully synchronized and performed by the FPGA controller. The conversion mode is Read After Convert and the data from each ADC is read serially to an off-board buffer.

15.8. Additional Circuits

The readout port of the ADC is protected from overload by a small buffer located on the board. The conversion start, serial clock and reset signals are distributed from the FPGA controller through fan-out drivers.

Additional status bits from the ADCs are monitored and those signal (BUSY and RDERR) are OR-ed together and sent to the FPGA controller.

A temperature and identification chip is also located on the board.

15.9. Functional Electrical Schematic

A diagram in Fig. 20 provides a functional description of the different stages of the signal-processing channel.

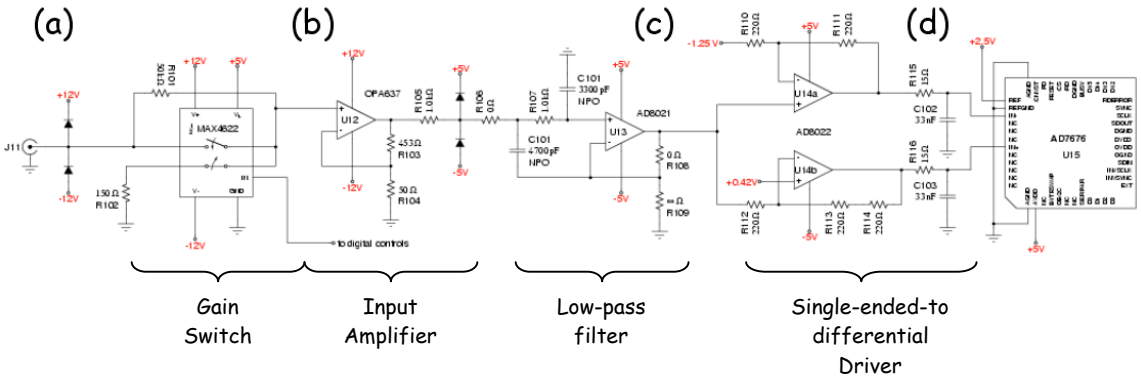


Fig. 20: UXO Signal-processing channel - Functional schematic

The gain was calculated to match the ADC input range. The following table shows the signal level at the marked locations of the circuit.

Signal Levels	(a)	(b)	(c)	(d)
Low Gain	± 12V	± 40mV	± 400mV	± 800mV
High Gain	± 50mV	± 50mV	± 500mV	± 1V
LSB (RMS)	2μV High Gain	2μV	20μV	40μV

Table 2: Signal Levels

15.10. Noise simulations

The signal level and the least significant bit (LSB) size (2μV RMS) at the input of the amplifier define the signal-to-noise ratio. Simulations were run to confirm the validity of the architecture and the effectiveness of the band limiting filter. The simulations were run in both high-gain and low-gain modes and the results are presented hereafter.

The simulation model described in Chapter 13.was modified to include the Low-Pass filter. The noise analysis was conducted with and without the filter. The input referred voltage noise density and the computed RMS equivalent for the latter are plotted in Figs. 21-24.

15.10.1. High Gain

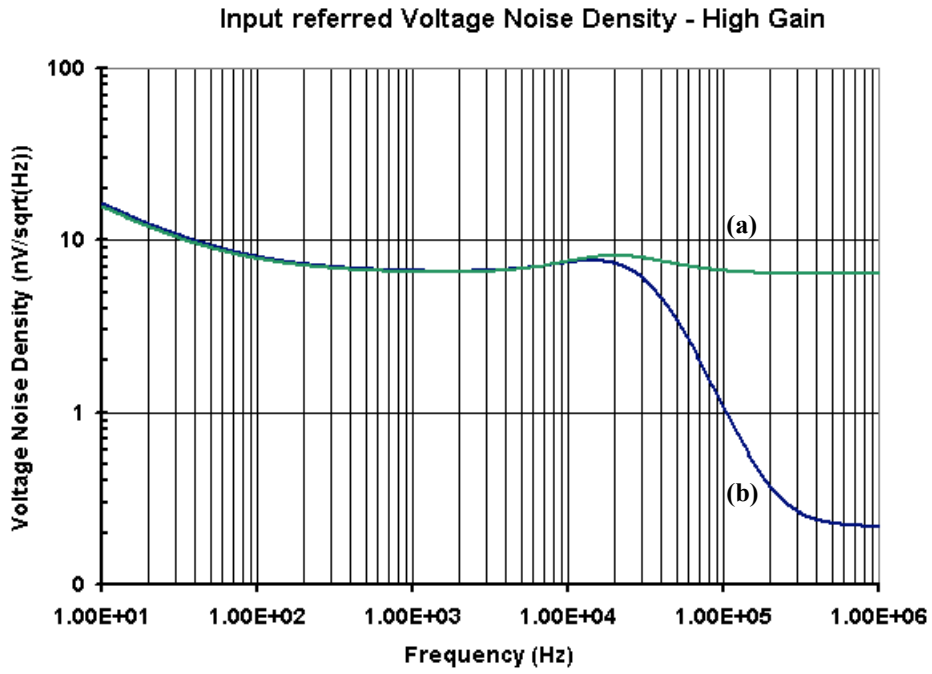


Fig. 21: HIGH GAIN - Simulated Amplifier Input Referred Voltage Noise Density
(a) Without Low-Pass Filter (b) With Low-Pass filter

The curve without the Low-Pass filter is identical to that of Fig. 10, exhibiting the resonance peak of the coil at 20 kHz. The 40 kHz Low-Pass filter reduces the noise-density at high frequency.

The input referred voltage noise density with the low-pass filter is integrated over frequency in order to compute the RMS equivalent value. The results are shown Fig. 22.

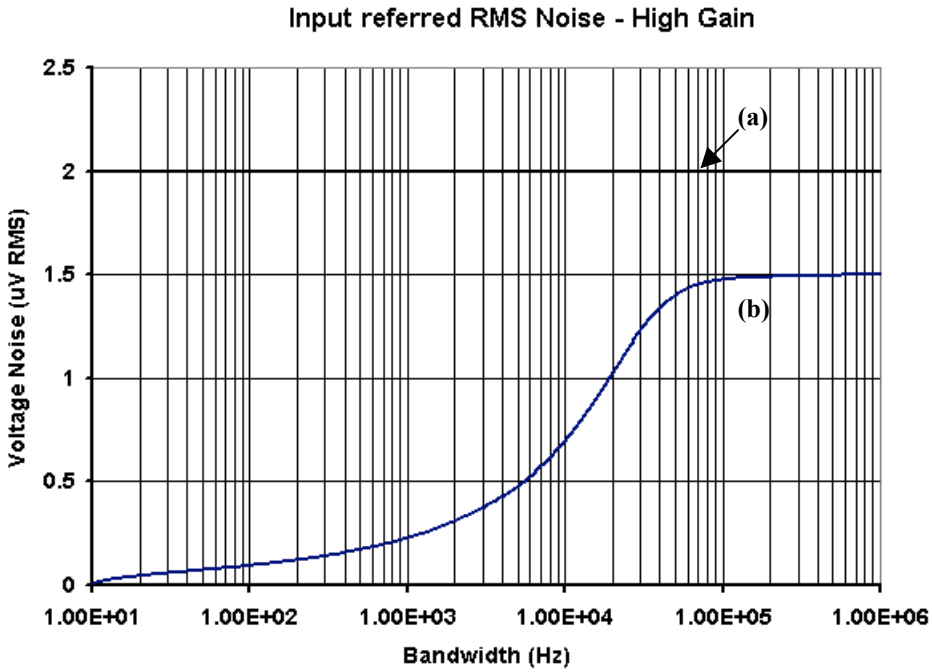


Fig. 22: HIGH GAIN – Amplifier's input equivalent RMS noise vs. integration bandwidth
(a) 2μV Reference Level (b) With Low-Pass filter

The integration of the input referred voltage noise density shows that the RMS value asymptotes to about 1.5μV for frequencies higher than 40 kHz, which is less than the requirement level of 2μV.

Low Gain

In a low gain mode, the 50 dB attenuator (resistive divider) is inserted in between the coil and the input of the amplifier. The main result is that the resonance peak of the coil at 20 kHz is completely attenuated (Fig. 23).

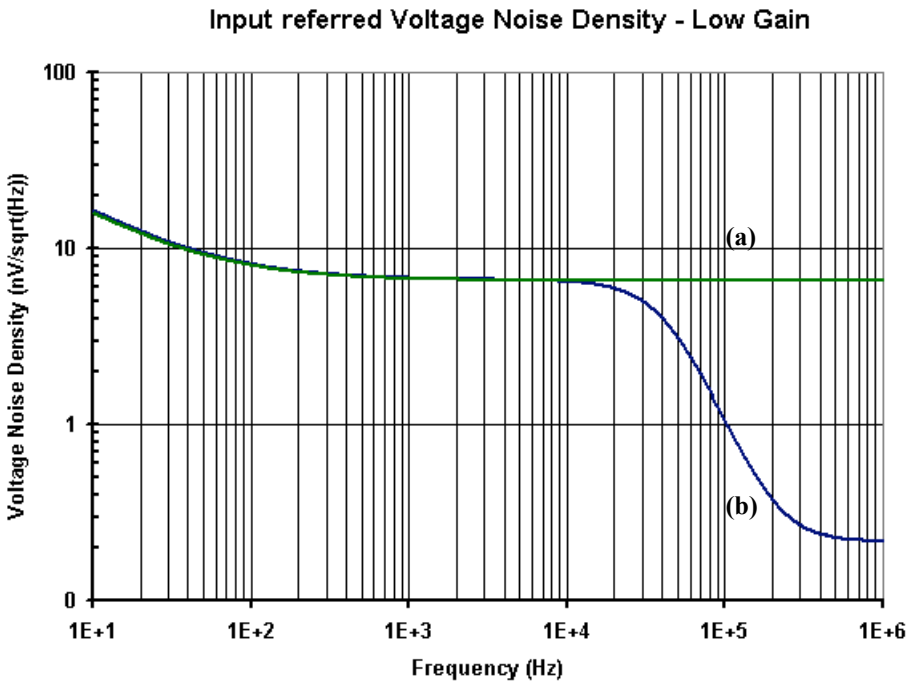


Fig. 23: LOW GAIN - Simulated Amplifier Input Referred Voltage Noise Density
(a) Without Low-Pass Filter (b) With Low-Pass filter

The input referred voltage noise density with the low-pass filter is integrated over frequency in order to compute the RMS equivalent value. The results are shown in Fig. 24.

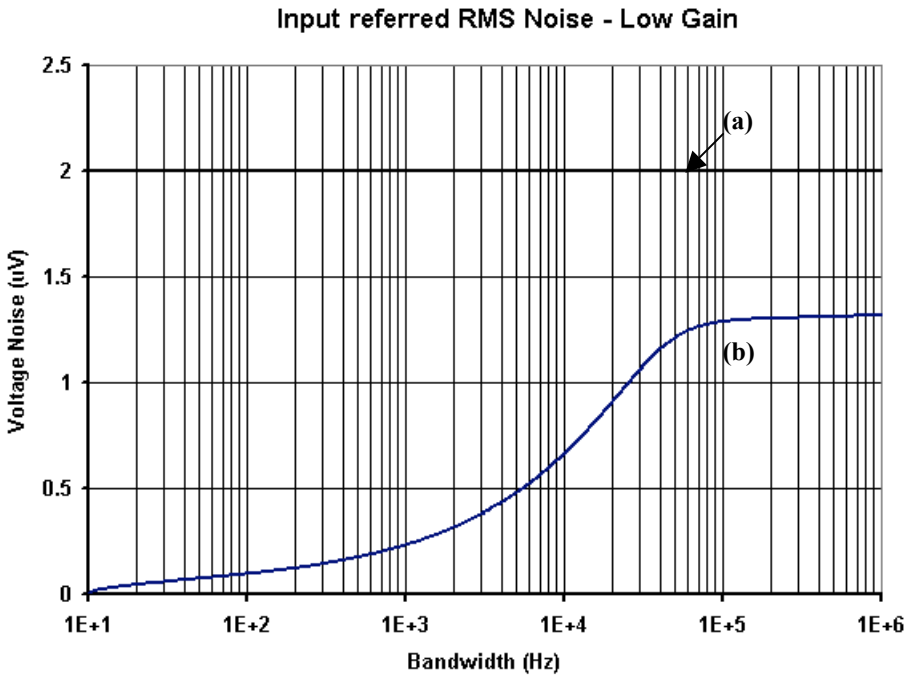


Fig. 24: LOW GAIN - Amplifier's input equivalent RMS noise vs. integration bandwidth
(a) 2μV Reference Level (b) With Low-Pass filter

In both cases – high and low gain modes – the RMS noise values computed from the results of simulations show that the signal-processing channel design meets the signal level requirements. The results are also reinforced by the measurements shown in Fig. 12.

16. Board layout

The board (Fig. 25) was laid out using the OrCAD Capture and Layout tools.

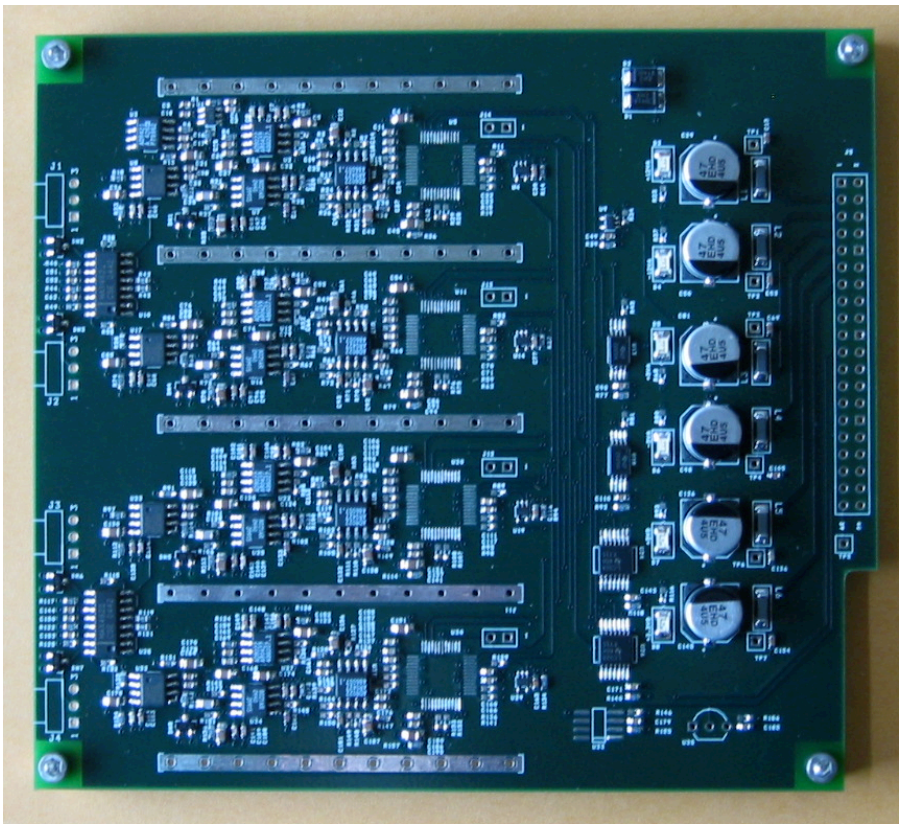


Fig. 25: UXO4CH Board Photograph (not fully assembled)

- Board dimensions: 5”x4.5”
- 6 layers, 2 routing layers, 3 power planes, 1 Ground plane
- 6 power supplies;
    - ± 12V, Analog: Gain switches and Input amplifiers
    - ± 5V, Analog: Low-Pass Filters, Single-ended-to differential Drivers and ADCs (+5VA only)
    - +5V,Digital: ADCs
    - +3.3V, Digital Logic

Estimated power consumption: 2W

17. Firmware development approach

Programming support for the UXO data acquisition system targets three separate devices, as shown in the block diagram of Fig. 4:

1. The FPGA (Xilinx XC4VLX25)

2. The USB interface chip (Cypress CY7C68013)

3. The laptop computer (Linux)

The FPGA programming is written in Verilog, simulated with Icarus Verilog, and synthesized using Xilinx XST. Some development takes place in VHDL; the synthesizer has a mixed-language mode, alternatively the VHDL can be machine translated to Verilog.

The USB interface chip is really an 8-bit microprocessor (8051 derivative), with high-speed interfaces to both the FPGA and the USB. One of its innovative features is the capability to boot from the USB at power on, simplifying the process of setting it up. The two high-speed interfaces between the FPGA and the USB are directly connected. In this configuration, the (relatively slow) microprocessor does not have to handle the data in each 512-byte packet, but is only used to set up the transfer between FPGA and the USB bus.

A free reference software design (GNU Radio) was adapted to our actual hardware. It programs the Xilinx FPGA over JTAG, provides access to the tune parameters within the FPGA over SPI, and sets up the high speed data transfer to the host. Data transfer has been successfully demonstrated at a sustained 33 MB/sec.

The host software at the receiving end of the USB data stream eventually needs to be integrated with a GUI and data analysis software. For the moment, our test software simply reads the data stream and stores it in a binary file for bulk analysis. Early example data is shown in Fig. 26.

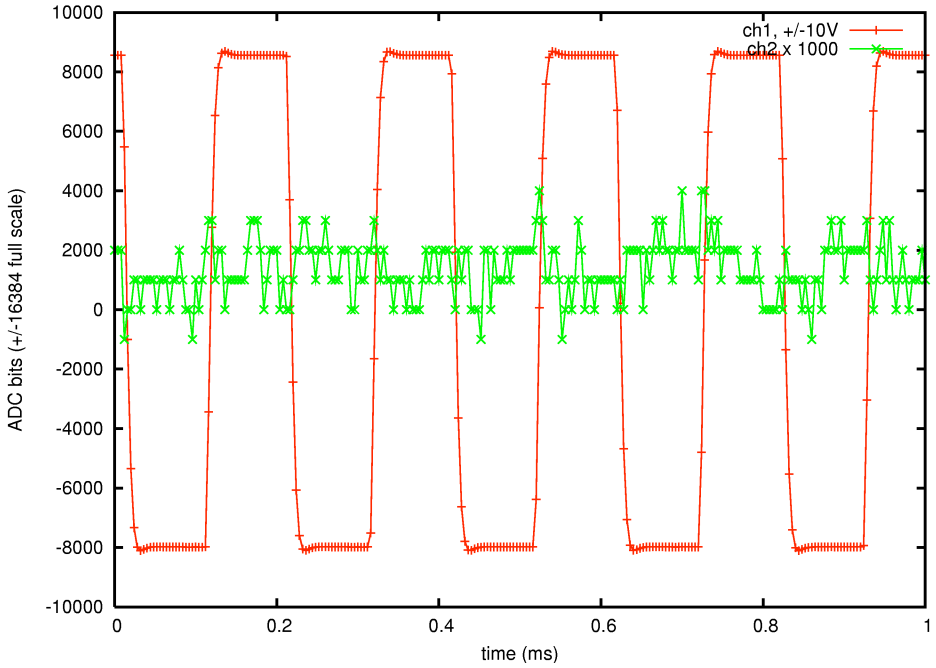


Fig. 26 –Example of data sampling from 16-bit system

With this setup we could acquire a noise spectrum, which is shown in Fig. 27. The analysis of these data determined that the intrinsic noise of the amplifier is as expected and matches the simulation results.

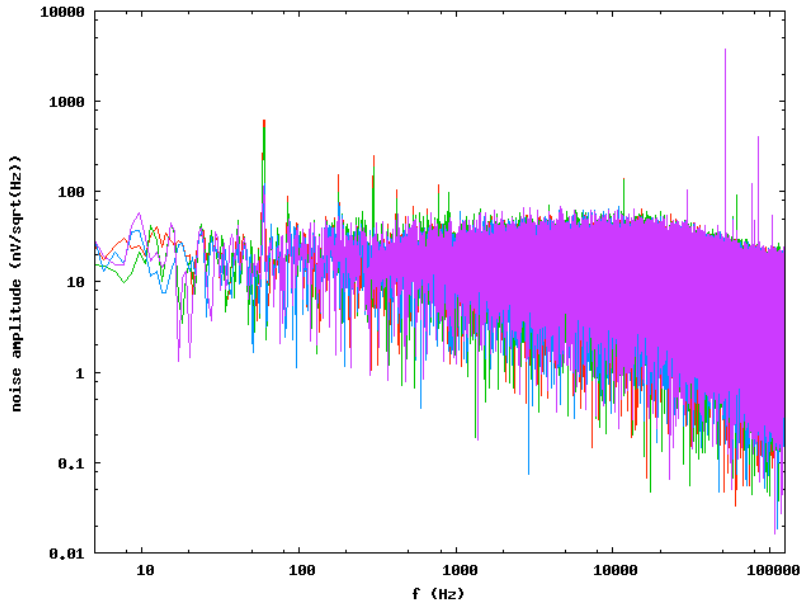


Fig. 27 – Noise spectrum acquired with the 16-bit system

Fig 28 shows a block diagram of the programming path for the main functions in the FPGA. As described earlier, the FPGA captures the input from the data acquisition chain, and processes it using the out-board RAM, which is dual data (DDR) synchronous dynamic random access memory (SDRAM). The date shown in this diagram is both at 16 and 32 bits.

Another important function of the FPGA is that of interfacing with the USB bus, which is used both to transfer the processed data to the main computer and also to receive the settings from it. This information can be used on a pulse to pulse basis to setup each acquisition according to the specific needs of the system. For example, if there is the need for high resolution scanning, then the FPGA can acquire data and transfer is to the main computer unprocessed, by slowing down the trigger to the excitation and data acqusition rate.

Last, the FPGA is used as the master to create the timing that will trigger all events, from pulsing to data acquisition and sampling.

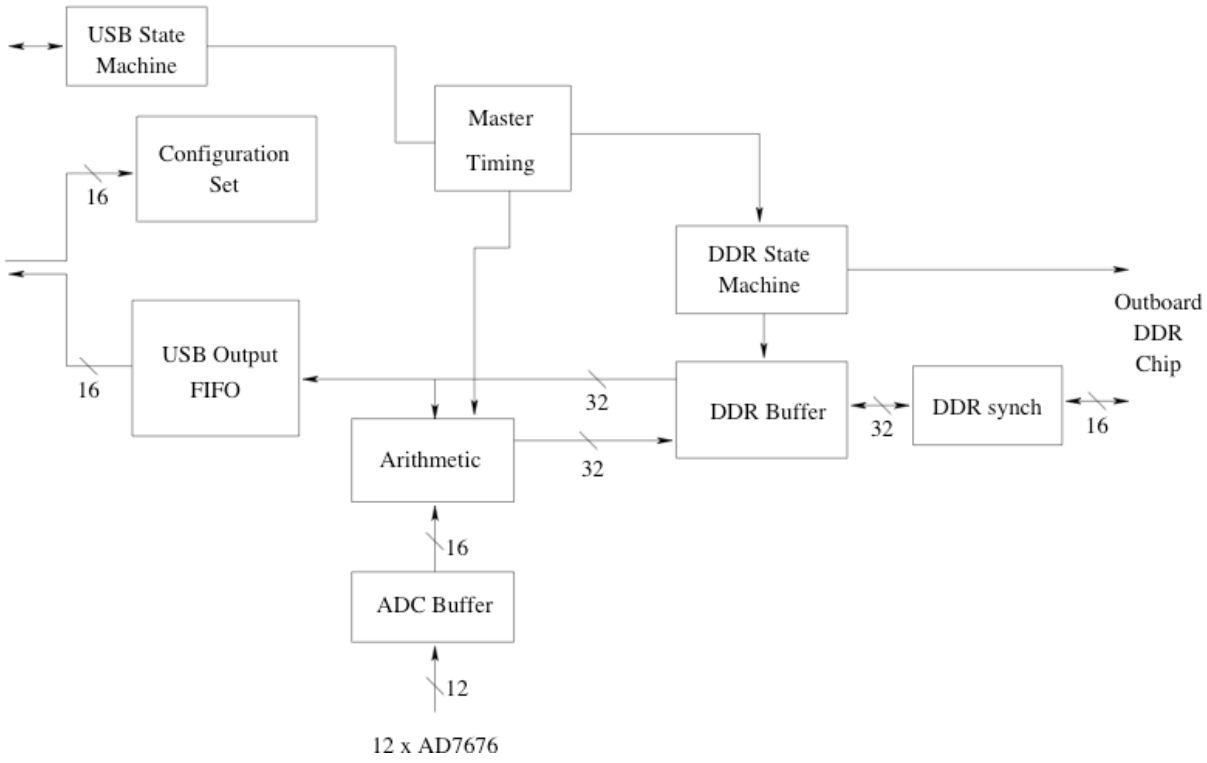


Fig. 28 – Firmware architecture block diagram

18. Cart design and description

Following the engineering approach adopted in the project, we took a stepwise approach toward building the cart. We started the design of the cart before the main parameters were fully defined; this allowed us to contribute to the feasibility study of the detector, and to understand and test the most important structural features of the cart.

The major parameters such as mass, resonant frequency and motion will emerge only after some experimental data accumulates and is analyzed. However, good estimates were developed as starting points and basic mechanical configurations and clearances for the coil package, electronics, and mechanical support systems (the cart) were proposed and implemented.

To expedite schedule and get to results faster, we developed the cart in parallel with the drive coils and sensors, and merged all components together. The following is a list of features currently implemented in the present design:

- Non-magnetic construction; plywood, plastic, rubber, glue
- Removable Boom
- Solid tires (foam-filled)
- Pneumatic tires (Add-on)
- Fiberglass leaf springs
- Pneumatic load levelers (Add-on)
- Double sphere universal joint coil interface
- Pneumatic Roll compensation and damping (Add-on)
- Aggressive Pitch damping (Add-on)
- More aggressive Roll compensation and damping. (Add-on)
- Expected to have a short, useful life. Iterated quickly into obsolescence
- It fits through the lab door

The present design was generated by utilizing a full 3D CAD system and modern wire-jet fabrication machines that allow for an easy, direct transfer of the drawings to the machine and a very quick turn around time. This design has been tested for vibration damping, which was found to be resonant at less than 1 Hz and to damp in about one cycle. The following is a set of images from the 3D CAD design of the cart, illustrating the design and assembly sequence of the cart.

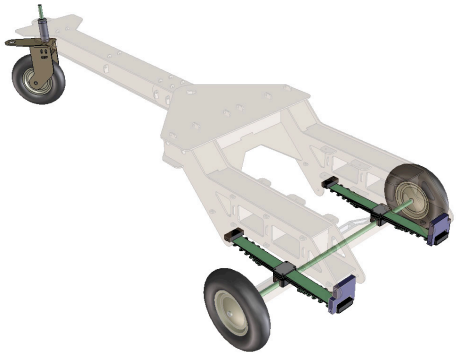


Fig.29 – Cart spring system

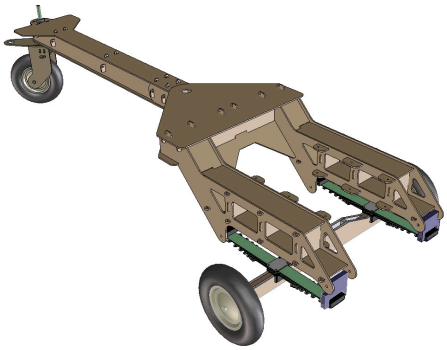


Fig. 30 – Cart structure

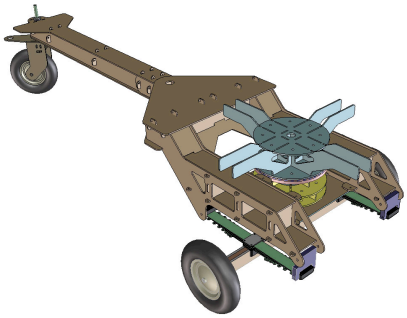


Fig. 31 – Detector support

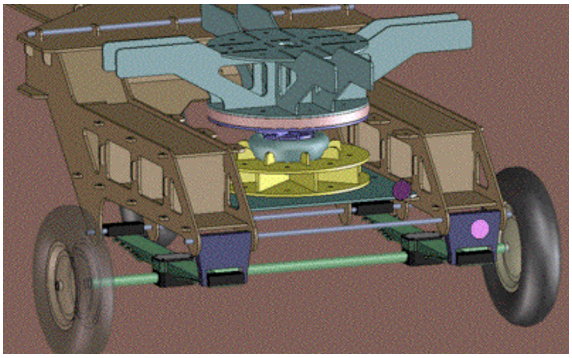


Fig. 32 – Detector damping system

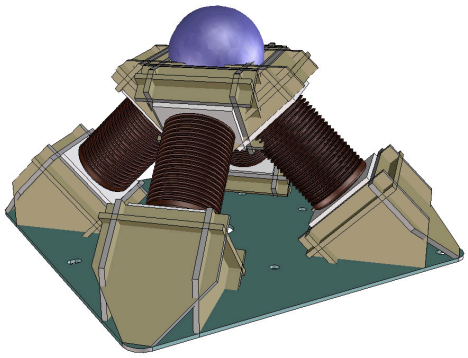


Fig. 33 – Alternate damping design

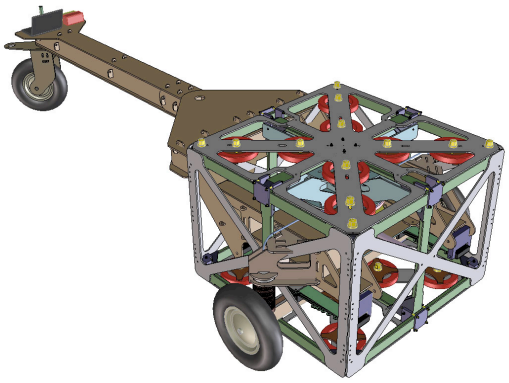


Fig. 34 – Final assembly

19. Appendix I - Battery lifetime estimate

UXO Battery lifetime

2/25/2005 Larry Doolittle

Defining:

T	battery lifetime
m_B	mass of battery
m_C	mass of coil
E	Energy density of battery
ρ	resistivity of coil material
σ	density of coil material
D	duty factor
$\mathcal{n}$	number of turns
ℓ	length (perimeter) of coil
I	peak current in coil
R	resistance of coil
A	cross sectional area of one turn of coil

we can express:

$$T = \frac{Em_B}{D\frac{1}{2}I^2R}$$

$$R = \frac{\mathcal{n}\ell}{A}\rho = \frac{(\mathcal{n}\ell)^2}{m_C}\rho\sigma$$

$$T = m_B m_C \frac{E}{\rho\sigma}\frac{2}{D(\mathcal{n}\ell I)^2}$$

Note the neat division in that last equation into system design, technology selection, and electromagnetic design terms.

E ~ 60 W · h/kg for Ni-MH rechargeable batteries.
ρσ ~ 7.7 x 10^{-5} Ω · kg/m^2 for Aluminum at 20˚˙C

D ~ 0.15 and $\mathcal{n}\ \ell$ I ~1900 A · m for the proposed UXO coil.

Combining the above numbers,

$$T = m_B\, m_C \cdot 2.8\ h/kg^2$$

so 1 kg of Ni-MH batteries can power a 1 kg Aluminum coil for 2.8 hours of operation. Sensible system designs will always have near equality of battery mass and coil mass. Operational lifetime scales as the square of the system mass.

One can consider three axes as independent of each other, and only combine the batteries later out of practical concerns. In that case, the duty factor for each battery/coil pair is effectively 0.05, so a combined three 3 kg of batteries and 3 kg of coils will last 8.4 hours.

Two robotcombat.com PN-3200N-24 packs of 20 sub-C cells (nominal 24V) weigh 1.2 kg each, 2.4 kg combined. They are in-stock for US $100 each. With three matching 0.8 kg coils, the (4.8 kg total) three-axis system should run for 5.4 hours.